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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Applicati n N .	Applicant(s)	
	10/763,164	LEE, CHAN-SUK	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/763164 Attorney's Docket #: 2557-000200/US
Filing Date: 1/26/2004; claimed foreign priority to 2/20/2003

Applicant: Lee

Examiner: Alexander Williams

Applicant's Amendment filed 3/8/06 has been acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-12, 14-17, 19 and 21 are rejected under 35 U.S.C. § 102(e) as being anticipated by Mess et al. (U.S. Patent # 6,900,528 B2).

1. Mess et al. (figures 1 to 29) specifically figures 13 and 14 show a stacked semiconductor package **50**

comprising: a first semiconductor chip **(60A)**; a second semiconductor chip **(60B)** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed and at least one bottom corner of the second semiconductor chip is exposed **(72)**; at least one first conductor **(wire 62 electrically connecting 60A to 60B)** electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and at least one second conductor **(wire 62 electrically connecting 60B to 66 on 70)** electrically connecting the second semiconductor chip to a frame **70.**

2. The package of claim 1, Mess et al. show wherein the first conductor electrically connects at least one bond pad **(54A pad on 60A)** on the first semiconductor chip with at least one bond pad **(54B pad on lower bottom chip 60B)** on the second semiconductor chip.

4. The package of claim 3, Mess et al. further comprising: a chip package structure dsupported by the frame **70**, the chip package structure including at least the first and second semiconductor chips **60A,60B**; and at least one second conductor **62** electrically connecting the differently positioned bond pad to the frame.

5. The package of claim 4, Mess et al. show wherein the second conductor **62** electrically connects the differently positioned bond pad **58** to a bond pad on the frame **(66 on 70)** (figures 13 and 14).

6. The package of claim 1, Mess et al. show wherein a plurality of first conductors **(62 connected to the top of 60A to the top of 60B)** electrically connect the exposed portion of the first semiconductor chip to the second semiconductor chip, the plurality of first conductors not extending beyond a periphery of the first semiconductor chip.

7. The package of claim 6, Mess al. further comprising: the plurality of first conductors **(62)** electrically connecting a plurality of bond pads **54A** on the first semiconductor chip to a first plurality of bond pads **54B** on the second semiconductor chip.

8. The package of claim 7, Mess et al. show wherein the plurality of bonds pads **54A** on the first semiconductor chip are arranged adjacent to an edge of the first semiconductor chip, and the first plurality of bond pads **54B** on the second semiconductor chip are arranged adjacent to an edge of the second semiconductor chip, the edge of the second

semiconductor chip corresponding to the edge of the first semiconductor chip.

9. The package of claim 8, Mess et al. further comprising: a redistribution pattern **62** electrically connecting the first plurality of bond pads **54A** on the second semiconductor chip to a second plurality of bond pads **54B** on the second semiconductor chip, the second plurality of bond pads arranged adjacent to a different edge of the second semiconductor chip (see figures 13 and 14).

10. The package of claim 7, Mess et al. further comprising: a redistribution pattern **62** electrically connecting the first plurality of bond pads **54A** on the second semiconductor chip to a second plurality of bond pads **54B** on the second semiconductor chip (see figures 13 and 14).

11. The package of claim 10, Mess et al. further comprising: the frame **70** supporting a chip package structure, the chip package structure including at least the first **60A** and second **60B** semiconductor chips; and a plurality of second conductors **62** electrically connecting the second plurality of bond pads on the second semiconductor chip to the frame (see figures 13 and 14).

12. The package of claim 11, Mess et al. show wherein the frame **70** is one of a printed circuit board and a flexible substrate.
14. The package of claim 13, Mess et al. further comprising: a sealing resin **84** sealing the first and second semiconductor chips, the redistribution pattern, the first and second plurality of conductors, and a portion of the frame.

15. The package of claim 11, Mess et al. show wherein the plurality of first and second conductors **62** are bonding wires.

16. Mess et al. (figures 1 to 29) specifically figures 13 and 14 show a stacked semiconductor package **50** comprising: a first semiconductor chip **60A;** a plurality of intermediate semiconductor chips **(N is 0 so not needed)** n, where n >= 0, each intermediate semiconductor chip stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip and at least one bottom corner of each intermediate chip is exposed; a second semiconductor chip **60B,** wherein when the expression n > 0 is satisfied, the second semiconductor chip is stacked offset over the intermediate semiconductor chips such that a portion of each intermediate semiconductor chip and at least one bottom corner of the second semiconductor chip are exposed, and when the expression n = 0 is satisfied, the second semiconductor chip is stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip and the at least one bottom corner of the second semiconductor chip are exposed; at least one first conductor **62** electrically connecting the exposed portions of the first and intermediate semiconductor chips to the second semiconductor chip, the first

conductor not extending beyond a periphery of the first semiconductor chip; and at least one second conductor **62** electrically connecting the second semiconductor chip to a frame **70**.

17. The package of claim 16, Mess et al. show wherein a plurality of first conductors electrically connect bonding pads on the exposed portions of the first, second and third semiconductor chips to a first plurality of bonding pads on the fourth semiconductor chip, the first conductors not extending beyond a periphery of the first semiconductor chip.

19. The package of claim 1, Mess et al. show wherein the first and second semiconductor chips are a same type of chip.

21. Mess et al. (figures 1 to 29) specifically figures 13 and 14 show a method for fabricating a stacked semiconductor package **50**, comprising: forming a stacked chip package **61** including at least a first semiconductor chip **60A** and a second semiconductor chip **60B** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip and at least one bottom corner of the second semiconductor chip is exposed; electrically connecting the exposed portion of the first semiconductor chip to the second

semiconductor chip using at least one conductor **(62)** such that the conductor does not extend beyond a periphery of the first semiconductor chip; and electrically connecting the second semiconductor chip to a frame **70.**

[0058] With reference to the drawings of drawing FIGS. 12, 13 and 14, which describe an embodiment of the instant invention, a semiconductor device 50 having a multi-chip module (MCM) type of configuration comprises two semiconductor dice 60A and 60B as a stack 61. This configuration is particularly appropriate to flash memory packages in which the die circuits are connected in parallel. In this configuration, the semiconductor dice 60A, 60B have essentially identical circuits and have upwardly facing active surfaces 52A, 52B with bond pads 54A, 54B along one edge 56A, 56B of each active surface, respectively. The bond pads of each semiconductor die 60 are collectively designated as a "field" 55 of bond pads. Each semiconductor die 60A, 60B has a length dimension 104 and a width dimension 106 which may be equal or unequal thereby making the die 60A, 60B have different physical sizes and shapes.

[0059] Semiconductor die 60A is shown attached to a substrate 70 by adhesive layer 78. The adhesive layer 78 may be any adhesive capable of bonding a reverse surface 72 of a die 60 to the active surface 52 of another semiconductor die or to a top side 66 of a substrate 70. Semiconductor die 60B is stacked on top of semiconductor die 60A and joined to it by thin adhesive layer 78. Semiconductor die 60B is offset from semiconductor die 60A along Y-axis 76 a distance 82 which exposes the field 55 of bond pads 54A. The offset distance 82 may be the shortest distance which permits reliable use of a wire bonding tool, not shown, to bond conductors such as bond wires 62 to the bond pads 54A. Thus, bond pads 54A, 54B are joined by fine metal bond wires 62 or other conductive members to conductive, e.g., metallization areas 58 on the top side 66 of substrate 70. If so dictated by the design of the device 50, certain bond pads 54A and 54B may also be conductively connected to each other, i.e., on the same semiconductor die 60A or 60B, or from semiconductor die 60A to semiconductor die 60B.

[0060] In these figures, the substrate 70 is pictured as a circuit board or memory card substrate or multimedia card substrate, for example. This example is shown with solder balls 64 on its reverse side 68 although other configurations of electrical connections may be used.

[0061] A controlled thickness thermoplastic or other type of adhesive may be used in adhesive layers 78 to join the semiconductor dice 60A and 60B to each other, and semiconductor die 60A to the substrate 70.

[0062] The bond pads 54A and 54B of dice 60A and 60B, respectively, are joined to metallization or other conductive areas 58 on the substrate 70 by thin bond wires 62. Typically, the bond wires 62 have a diameter of about 0.001 inch and are formed of a metal such as aluminum or gold, or alloys thereof. The preferred method of bonding the bond wires 62 to the bond pads is known as ultrasonic ball bonding, which forms a low-loop wire bond which is less than the Z-dimension of a semiconductor die 60. Likewise, in a preferred method, ultrasonic "wedge" bonds of wire are formed at the substrate metallization 58.

[0063] In general, semiconductor devices are encapsulated in a protective package to protect the die surfaces, metallization and wires from damage. As depicted in drawing FIGS. 12 through 14, edges of an exemplary equiangular encapsulating enclosure are defined by lines 84. The encapsulant material may be a polymer, ceramic or other protective material. As shown, the completed, i.e., packaged device 50 may be formed to have a low profile vertical (Z) dimension 86 (excluding solder balls 64) which is less than prior stacked device heights, because thick intervening layers of adhesive are not required between adjacent semiconductor dice 60.

[0064] A stack 61 of two or more offset semiconductor dice 60 may also be formed on a lead frame 94, as depicted in an example in drawing FIG. 12A. The lead frame 94 is typically formed from a material such as copper, copper alloys, iron-nickel alloys, or the like. Other materials, such as TAB tape, could be used in accordance with this invention as well. The lead frame 94 is shown with opposing runners 96, a central paddle 98, and leads 102A and 102B to which wires are attached. The lead frame 94 has alignment mechanisms 100 such as precisely positioned marks

or holes, for precise positioning of the lead frame 94 during operations such as die bonding and wire bonding where alignment is critical. In this example, semiconductor die 60A is attached to a paddle 98 of lead frame 94 with a thin adhesive layer, not shown. The paddle 98 serves as a substrate to support the stack 61. Semiconductor die 60B is then attached to overlie a major portion of semiconductor die 60A, wherein the die edge 56B along which bond pads 54 are positioned is offset a distance 82 from the die edge 56A of the lower semiconductor die 60A, to expose the bond pads 54. As shown, conductive bond wires 62A are connected from bond pads 54B of semiconductor die 60A to appropriate leads 102A. Likewise, bond wires 62B are connected from bond pads 54B to leads 102B. Alternatively, TAB bonding or other bonding methods may be used. As illustrated in drawing FIG. 12B, the semiconductor die 60B is of smaller size than that of semiconductor die 60A. Further, as illustrated in drawing FIG. 12C, the semiconductor die 60B is of larger size than semiconductor die 60A having three sides of the semiconductor die 60B overhanging the semiconductor die 60A.

[0065] In the embodiment of drawing FIGS. 12 through 14, both of the semiconductor dice 60A, 60B have their bond pads 54A, 54B oriented in the same direction so that they are connected by bond wires 62 to metallization areas 58 on the same side of the device 50. However, the semiconductor die orientation and other factors, such as semiconductor dice having different sizes and dimensions, may be changed to suit a particular application. Thus, major design factors affecting the stacked offset multiple semiconductor die device 50 include the number of semiconductor dice 60 in the stack 61, die dimensions, number of die edges 56 along which bond pads 54 are arrayed, offset direction(s), offset distance 82 and rotation angle of each semiconductor die 60 relative to the semiconductor die 60 just below.

Claims 13, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mess et al. (U.S. Patent # 6,900,528 B2) in view of Kato et al. (U.S. Patent Application Publication # 2002/0140107 A1).

Mess et al. show the features of the claimed invention as detailed above, but fail to explicitly show the frame includes a die pad portion supporting the chip package structure and an

inner lead portion to which the plurality of second conductors are electrically connected and a redistribution pattern electrically connecting the first plurality of bond pads on the second semiconductor chip to a second plurality of bond pads on the second semiconductor chip.

Kato et al. show a semiconductor device. Specifically, Kato et al. (figures 1 to 35) specifically figures 14 and 15 show a stacked semiconductor package **10E** comprising: a stacked chip structure including an upper semiconductor chip **12A** and at least one lower semiconductor chip **11A** disposed under at least a portion of the upper semiconductor chip; and a redistribution pattern **51** redistributing a first plurality of bond pads **18A** on the upper semiconductor chip to a differently positioned second plurality of bond pads **18B** on the upper semiconductor chip, the first plurality of bond pads **18A** being electrically connected with the lower semiconductor chip **11A**, wherein the frame includes a die pad portion supporting the chip package structure and an inner lead portion to which the plurality of second conductors are electrically connected (**see paragraph [0013]**) and further comprising: a redistribution pattern **51** electrically connecting the first plurality of bond pads **18B** on the second semiconductor chip **12A** to a second plurality of bond pads **18A** on the second semiconductor chip (see figures 14 and 15) for purpose of providing improved internal wiring connection between semiconductor chips.

13. The package of claim 11, the combination with Kato et al. show wherein the frame includes a die pad portion supporting the chip package structure and an inner lead portion to which the

plurality of second conductors are electrically connected (see paragraph [0013]).

18. The package of claim 17, the combination with Kato et al. further comprising: a redistribution pattern **51** electrically connecting the first plurality of bond pads **18B** on the second semiconductor chip **12A** to a second plurality of bond pads **18A** on the second semiconductor chip (see figures 14 and 15).

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Kato et al.'s internal wiring connections to modify Mess et al.'s package for purpose of providing improved internal wiring connection between semiconductor chips.

Response

Applicant's arguments filed 3/8/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1, 16, 20 and 21" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED

STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,784,786,787,773,696,698,e23.172,e25.013,e23.176,e21.526,e25.011	6/24/05 11/5/05 5/17/06
Other Documentation: foreign patents and literature in 257/686,685,723,777,784,786,787,773,696,698,e23.172,e25.013,e23.176,e21.526,e25.011	6/24/05 11/5/05 5/17/06
Electronic data base(s): U.S. Patents EAST	6/24/05 11/5/05 5/17/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
5/18/06